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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Kazuya KAWAKAMI et al.
Serial No.:	10/084,943
Filed:	March 1, 2002
For:	METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND SEMICONDUCTOR MANUFACTURING APPARATUS
Group:	2812
Examiner:	G. Peralta

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REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 2, 2004

Sir:

In response to the Office Action dated August 1, 2003, the period of response for which extension is requested by the attached Petition for Extension of Time, Applicants respectfully request reconsideration for the reasons set forth below.

Briefly, the present invention is directed to a method of manufacturing semiconductor integrated circuit devices involving a manufacturing apparatus that includes a plurality of chambers. An example of such an apparatus is shown, for example, in Fig. 1 of the specification in which a plurality of processing chambers 3A-3D are provided to perform a plurality of processes on wafers which are transported by a robot arm 4 between the different process chambers. The

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unprocessed wafers 6 are stored in load-lock chambers 2 and are removed for processing in the manner shown in Fig. 2 (e.g. see page 15, line 19 et seq). As shown in Figs. 1 and 3, in addition to the processing chambers 3A-3D, a transport chamber 1 is also provided. The processed wafers 9 are moved through the transport chamber 1 between the different process chambers 3A-3D.

As discussed on page 16, line 9 et seq:

> "In the transport chamber 1, a wide-angle lens 7 (photographing unit) such as a fish-eye lens is provided near the gate to the process chamber 3A, which makes it possible to photograph the entire image of a wafer 9 right after being processed in the process chamber 3A on the robot arm 4 from the top of the transport chamber 1 by the use of a camera 8 (photographing unit) such as CCD (charge coupled device) camera."

Following this, a step of processing the entire image which has been photographed is performed as discussed beginning on page 17, line 1. Fig. 4 provides a flowchart of the steps of processing of the entire image of the wafer 9 photographed by the camera 8. In particular, as discussed on page 17, line 15 et seq:

> "The photographed entire image (first image) of a wafer 9 is transmitted from the camera to a discrimination unit 10. Thereafter, signal processing (image processing) is performed thereto by the discrimination unit 10."

Following this, as discussed on page 17, line 24 et seq signal processing is performed by comparing the actual image which has just been taken of the wafer 9 with the image of a wafer in which no breakage or cracks occur, in other words, a reference. As one example of such comparison, page 17, line 27 et seq notes:

> "When there is the breakage or the crack on the wafer 9, the color tone on the gray scale where the portion of the breakage or crack occurs is different from that of the other portion in the gray-scale image data. Therefore, it becomes possible to detect the presence of the breakage or crack."

Page 18, line 4 et seq continues in describing that when no breakage or crack is detected, the wafer is transported to the next process chamber 3B. On the contrary, if a breakage or crack is detected, the discrimination unit 10 transmits an error signal to stop the operation in the transport chamber 1 and in the processing chambers.

In summary, the present invention provides a wafer inspection technique based on photographing an entire image of a wafer and processing the photographed image so that damage such as breakage or a crack on the wafer can be detected without fail in a multi-chamber apparatus (e.g. see page 5, line 28 et seq and page 43, line 16 et seq).

Reconsideration and allowance of claims 1-13 over the cited references to Theriault (USP 6,530,732), Farber (USP 6,232,134) and Yasuyuki (JP 1995-58175) is respectfully requested.

Claims 1-13 define the method of manufacturing a semiconductor integrated circuit device in a semiconductor manufacturing apparatus having a plurality of chambers from a number of different perspectives. However, in each instance, a method is described in which an image is obtained of a flat entire image of a semiconductor wafer after performing a first process to the wafer in a first chamber from among a plurality of chambers. All of claims 1-13 also define using the flat entire image of the semiconductor wafer to determine the condition of the wafer by

examining the flat entire image of the wafer. Following this processing of the image to determine whether the wafer is damaged, the method defined in these claims determines whether the wafer is transferred to a second chamber for a second process or the operation of the manufacturing apparatus is stopped due to a determination of some sort of damage.

As such, all of the present claims 1-13 define an overall combination of steps performed in conjunction with a multi-chamber semiconductor manufacturing apparatus. As discussed on page 2, line 22 et seq., multi-chamber semiconductor manufacturing devices are subject to damage of the wafers due to either damage caused in the transportation process of the relatively delicate wafers or thermal stress applied to the wafers during the individual processes themselves. To address this, all of the present claims define at least the steps of:

1. performing a first process on wafer in a first chamber of the multi-chamber semiconductor manufacturing apparatus;
2. photographing a flat entire image of the semiconductor wafer after the first process has been performed, but prior to performing a second process in a second chamber;
3. determining whether the wafer has experienced some damage following the first process or the transportation of the wafer, which determination is based on processing the data from the flat entire image;
4. transporting the wafer to the next process if no damage is detected; and

5. stopping the operation of the semiconductor manufacturing apparatus if it is determined from the signal processing of the flat entire image that damage has, in fact, occurred to the wafer either in the first processing chamber or in the transporting operation.

It is respectfully submitted that none of the cited references teaches or suggests the overall combination of features set forth in the claims 1-13 of the present application. Quite to the contrary, as recognized in the Office Action, the references provide only isolated elements of the present invention, which must be combined and further modified to try to meet the overall combination of limitations set forth in claims 1-13. However, as will be discussed below, it is respectfully submitted that there is no motivation in the cited references themselves to make the modifications proposed in the Office Action. Quite to the contrary, the sole motivation for making such modifications would have to come from the present application itself. As set forth in the recent CFAC decision In re Lee 61 USPQ2d 1430:

> "The factual question of motivation is material to patentability, and cannot be resolved on subjective belief in unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "use that which the inventor taught against its teacher". (31 USPQ2d 1434).

However, it is respectfully submitted that, in the present instance, the Applicants own teaching have been used in formulating the rejection, directly contrary to the holding in the In re Lee decision.

Turning to the specifics of the rejection, the primary reference to Theriault simply discloses a multiple-chamber type semiconductor manufacturing apparatus utilizing one load lock chamber and a transporting chamber. The purpose of the invention in Theriault is to prevent damage to a wafer by thermal impact occurring when a wafer is transported from an external environment into the load lock chamber or when the wafer is transported from the load lock chamber to a processing chamber. As such, a cooling chamber is provided where the wafer is cooled. Although this multi-chamber type semiconductor manufacturing apparatus of Theriault may be of general interest to the present invention it is readily recognized in the Office Action that it certainly does not teach the combination of steps set forth in the present claims. As stated in page 2 in the last paragraph of the Office Action:

> "Theriault et al. discloses the claimed invention with the exception of obtaining flat entire image of the semiconductor wafer after performing the first process, determining the condition of the wafer by examining the flat entire image, and transporting the semiconductor wafer to the second chamber if the semiconductor wafer is determined to be in proper condition or stopping the operation if the wafer is determined to be in improper condition."

In other words, it is recognized in the Office Action that Theriault fails to teach or remotely suggest the fundamental features of the present invention which are utilized for detecting whether damage has occurred to the wafer or not and

controlling further processing based on this determination. In short, Theriault simply teaches which has already been admitted in the background of the invention, that is, that multiple-chamber processing apparatus has been known in the past. Beyond this, the reference offers absolutely nothing for solving the problem addressed by the present invention of detecting a damaged wafer and controlling the processing of the semiconductor manufacturing apparatus accordingly.

The secondary reference to Farber provides a particular technique to optically examine a charged wafer to measure charge distribution for purposes of monitoring wafer processing consistency and/or accuracy in a semiconductor manufacturing process. To this end, after a layer of dielectric is formed on a wafer, it is subject to plasma processing, resulting in a surface charge being induced on the wafer. As shown in Fig. 1 of Farber, the surface charge distribution is measured and compared with a known surface charge distribution pattern. Following this comparison, step 110 shown in Fig. 1 indicates that the process parameters are evaluated based on the results of the comparison. Details of the step 110 are provided in col. 6, line 58 et seq. As set forth with regard to step 110 in col. 6, the evaluation can determine "whether etching characteristics associated with the processing step being monitored are acceptable." They can also be used to determine whether changes need to be made to the etching process.

Again, while this may be of general interest to the present invention, it has absolutely nothing to do with the claimed steps of photographing a flat entire image after a first process has been performed in a first chamber to perform an evaluation to determine whether a wafer should be moved on to a second process chamber or

the operation should be stopped. Quite to the contrary, Farber simply represents an unrelated evaluation process utilized for adjusting processing parameters, and clearly provides no motivation whatsoever for modifying the primary reference to Theriault to arrive at the present claimed invention. Even if some motivation existed for combining Farber and Theriault, the end result would simply be an analysis of surface charge distribution patterns on wafers subjected to plasma processing for purposes of adjusting the etching operation. Clearly, this would be completely different from the features set forth in the present claims of photographing a flat entire image of a wafer after it has been processed in a first chamber and analyzing the flat entire image to determine whether damage has occurred to the wafer as a basis for determining whether the wafer should proceed to a second processing chamber in the multi-chamber apparatus or not.

The third reference to Yasayuki is discussed in the specification, for example, on page 3, lines 10-18. As discussed there, Yasayuki provides an inspection arrangement in which a wafer is photographed and the center of gravity of the wafer is detected by image processing of the picture image to permit movement of a wafer, even if it is broken, in such a manner that it is not dropped along the way. The only aspect of Yasayuki which has anything to do with the present invention is that it uses photography and image processing for some purpose. The specific purpose of Yasayuki for the photography and image processing is completely different from that of the present claimed invention. In particular, Yasayuki uses the photography and image processing to establish the center of gravity of the wafer to ensure that it can be transported without dropping. Again, there is no motivation whatsoever in

Yasayuki for modifying the primary reference to Theriault to arrive at the present claimed invention. Even if Yasayuki and the Theriault could be combined, the end result would be utilizing photography and image processing to prevent dropping of the wafers being processed in Theriault. This is completely different from the claimed method of photographing and analyzing the image data of a wafer after a processing operation has been carried out in a first chamber, and using the result of the analysis to determine whether to pass the wafer to a second processing chamber or to stop the operation of the multi-chamber semiconductor processing apparatus.

As set forth in the above discussion, the three references to Theriault, Farber and Yasayuki simply represent isolated teachings of general interest to the present invention. None of them provide the motivation for arriving at the claimed series of steps set forth in claims 1-13. Indeed, even if these references could be combined, the end result of the combination would have to be substantially further modified to arrive at the present claimed invention. In particular, even if the references were combined, none of them suggest the use of photography and image processing of a flat entire image of a semiconductor wafer after it has been subjected to a first processing operation in a first process chamber to determine whether the wafer should be passed along to a second processing chamber or the operation should be stopped. In essence, none of the references relied upon in the rejection deal with the problem of semiconductor wafers which can be damaged in the course of carrying out a processing operation in a first chamber or transporting the wafer to and from the various processing chambers. Therefore, it is urged that the

references themselves lack the necessary motivation for the substantial modification of Theriault which would be required to arrive at the claimed invention.

With regard to this matter, the Examiner's attention is also directed to the CAFC decision of In re Fine 5 USPQ2d 1596 (Fed. Cir. 1998). As stated in that case:

> "Because neither Warnick nor Eads, alone or in combination, suggest the claimed invention, the Board erred in affirming the Examiner's conclusion that it would have been obvious to substitute the Warnick oxide detector for the Eads sulfur dioxide detector in the Eads system. The Eads and Warnick references disclose, at most, that one skilled in the art might find it obvious to try the claimed invention. But whether a particular might be 'obvious to try' is not a legitimate test to patentability." 5 USPQ2d at 1599.

And yet, in the present instance, it is respectfully submitted that the only basis for arriving at the claimed invention would be exactly such an "obvious to try" rationale. In the first place, there is no motivation for combining the individual teachings of Farber and Yasayuki with Theriault to modify the general teaching of multi-chamber processing set forth in Theriault in the first place. Theriault is concerned with a completely different problem, resolved by providing a cooling chamber. Farber is directed to resolving a problem in plasma etching by measuring surface charge distribution patterns and adjusting the etching parameters accordingly. Yasayuki is concerned with preventing droppage of broken wafers. None of these references are concerned with the problem of the present invention that damage can occur during processing a wafer in a multi-chamber environment or in transporting a wafer

between the multiple chambers. As such, the only motivation for combining would come from Applicants' own teachings.

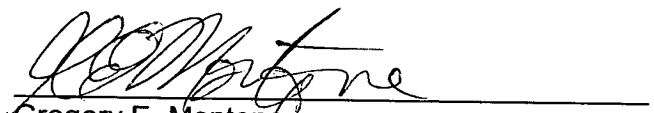
Beyond this, even if the references could be combined, the result would be completely different, as discussed in detail above. Combining Theriault and Farber would merely result in evaluating surface charge distribution patterns in Theriault after an etching process to determine whether the etching parameters needed to be modified. Combining Yasayuki would simply result in ensuring that broken wafers are not dropped. No basis whatsoever exists in any of the references for the actual claim steps of using photography and image processing to determine whether or not the wafers should be moved to a second process after a first process has been performed, or whether the overall operation should be stopped. Therefore, it is urged that the rejection of claims 1-13 should be removed, and such action is earnestly solicited, together with the allowance of claims 1-13.

If the Examiner believes that there are any issues which can be resolved by way of either a telephone or personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (referencing attorney docket no. 500.41231X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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